Claims

What is claimed is:

1. A processor comprising:

a packet analyzer; and

first memory circuitry associated with the processor and operatively coupled to the packet analyzer;

wherein the packet analyzer is operative to at least partially analyze one or more packets received by the processor in order to determine for a given one of the packets a portion of the packet to be stored in the first memory circuitry, the portion of the given packet when stored in the first memory circuitry thereby being accessible for subsequent processing within the processor without requiring access to second memory circuitry associated with the processor and configured to store substantially the entire given packet.

2. The processor of claim 1 wherein the processor is configured to provide an interface between a network from which the packets are received and a switch fabric.

3. The processor of claim 1 wherein the first memory circuitry comprises an internal memory of the processor and the second memory circuitry comprises an external memory of the processor.

4. The processor of claim 3 wherein the portion of the packet to be stored in the internal memory comprises a designated portion of a header of the packet.

5. The processor of claim 3 wherein the packet analyzer at least partially analyzes each of the packets received from a network and determines for each of at least a subset of the packets a particular portion of the packet to be stored in the internal memory.

6. The processor of claim 3 wherein the packet analyzer is configured to utilize a value stored in a register of the processor to determine the portion of the given packet to be stored in the internal memory.

7. The processor of claim 6 wherein the register comprises one of a plurality of registers which implement a look-up table accessible to the packet analyzer.

8. The processor of claim 7 wherein the look-up table includes a plurality of entries, each of at least a subset of the entries including packet categorizing information and an associated number of blocks of the packet to be stored in the internal memory.

9. The processor of claim 8 wherein the packet categorizing information comprises a port number specifying a port associated with the processor at which one or more of the packets may be received.

10. The processor of claim 8 wherein the packet categorizing information comprises a packet identifier specifying a particular packet flow.

11. The processor of claim 8 wherein the associated number of blocks comprises a predetermined number of blocks indicating for the given packet that substantially the entire packet is to be stored in the internal memory.

12. The processor of claim 6 wherein the stored value is updatable for each of at least a subset of the packet in a sequence of the received packets.

13. The processor of claim 6 wherein the same stored value is utilizable for multiple ones of the received packets to determine corresponding portions of the multiple packets to be stored in the internal memory.

14. The processor of claim 6 wherein the value stored in the register is storable therein under control of a host processor operatively coupled to the processor.

15. The processor of claim 14 wherein the host processor is coupled to the processor via a peripheral component interconnect (PCI) bus.

16. The processor of claim 3 further comprising a register which under control of the packet analyzer stores packet categorizing information for the given packet and a corresponding indication of the portion of the packet to be stored in the internal memory.

17. The processor of claim 3 further comprising a memory controller operatively coupled to the packet analyzer, the memory controller controlling the storage of the portion of the given packet in the internal memory.

18. The processor of claim 1 wherein the processor comprises a network processor.

19. The processor of claim 1 wherein the processor is configured as an integrated circuit.

20. A processing system comprising:

a processor; and

an external memory operatively coupled to the processor;

the processor further comprising:

a packet analyzer; and

an internal memory operatively coupled to the packet analyzer;

wherein the packet analyzer is operative to at least partially analyze one or more packets received by the processor in order to determine for a given one of the packets a portion of the packet to be stored in the internal memory, the portion of the given packet when stored in the internal memory thereby being accessible for subsequent processing within the processor without

requiring access to the external memory, the external memory being configured to store substantially the entire given packet.

21. A method for use in processing packets in a processor, the method comprising the steps of:

at least partially analyzing one or more packets received by the processor in order to determine for a given one of the packets a portion of the packet to be stored in first memory circuitry associated with the processor; and

storing the portion of the given packet in the first memory circuitry, the portion of the given packet thereby being accessible for subsequent processing within the processor without requiring access to second memory circuitry associated with the processor and configured to store substantially the entire given packet.